

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Fried et al.

Art Unit:

Serial No.:

Dkt. No.: BUR920010082US2

Filed:

Examiner:

Title: MULTIPLE-PLANE FINFET CMOS

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Preliminary Amendment

Sir:

Kindly enter this amendment prior to initial examination

In the Specification:

Page 1, between lines 1 and 2, insert: --This application is a divisional of Serial No. 10/011,846; filed on 12/4/2001.--

Please amend the paragraph beginning on page 1, line 11, and extending through page 2, line 8 as follows:

The push for ever increasing device densities is particularly strong in complementary metal oxide semiconductor (CMOS) technologies, such as the in the design and fabrication of field effect transistors (FETs). FETs are the basic electrical devices of today's integrated circuits and are used in almost all types of integrated circuit design (i.e., microprocessors, memory, etc.). FETs may be formed on conventional substrates. For example, a conventional CMOS FET formed on a silicon wafer may include a gate oxide layer formed on the wafer, a gate formed on